2007 Litho ITRS Update

Lithography iTWG

December 2007

Outline

- Lithography Potential Solutions
- Variability Control
- Double Exposure / Patterning
- 2008 Outlook

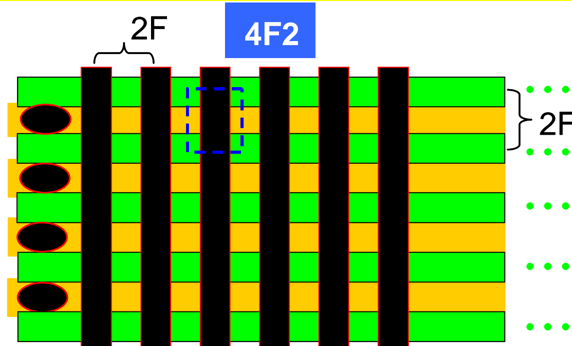
ITRS Working Group

- United States
  - Michael Lercel (Chair), Gene Fuller (Co-chair)
- Japan
  - Iwao Higashikawa (Chair), Takayuki Uchiyama (Co-Chair)
- Europe
  - Mauro Vasconi (Chair), Yves Rody (Co-chair)
- Taiwan
- Korea

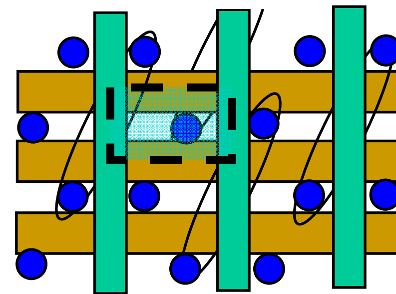
Driving Factors for Changes

- Flash roadmap half-pitch acceleration
- Exposure tool availability
  - EUVL: no beta tools until at least 2009
  - 193i high-index: new lens material for final lens element needed (2009+)
- Extensions of current technology
  - Double exposure / patterning

Typical NAND Flash cell
Can be manufactured at k_1<0.3



Typical DRAM cell
Not easily compatiable with k_1<0.3



Potential Solutions (2007 Update)

2007 2010 2013 2016 2019 2022
2008 2009 2011 2012 2014 2015 2017 2018 2020 2021 2023

DRAM 1/2 Pitch | 65nm

193nm immersion with water
193nm immersion double exposure / patterning

65
193 nm
193 nm immersion with water

Flash Half-pitch

45
45
193 nm immersion with water
193 nm immersion double patterning
Narrow options

32
32
193 nm immersion double patterning
EUV
193 nm immersion with other ...
materials
ML2, Imprint

193nm immersion double exposure / patterning
EUVL
193i+ with other fluids and lens materials
ML2, Imprint

22
EUV
Innovative 193 nm immersion
ML2, imprint, innovative technology
options

16
Innovative technology
Innovative EUV, ML2, imprint, Directed Self Assembly
Narrow options

193nm Litho – Numerical Aperture

Year of Production	2007	2008	2009	2010	2011	2012	2013	2014	2015
DRAM ½ pitch (nm)	**65**	**57**	**50**	**45**	**40**	**36**	**32**	**28**	**25**
Flash ½ pitch (nm)	*54*	*45*	*40*	*36*	*32*	*28*	*25*	*23*	*20*
NA required for Flash, single exposure	**1.01**	**1.20**	**1.35**	**1.52**	**1.70**	**1.91**			
NA required for Logic, single exposure	**0.91**	**1.04**	**1.20**	**1.38**	**1.54**	**1.73**	**1.94**		
NA required for Flash, double exposure	**0.72**	**0.86**	**0.96**	**1.08**	**1.22**	**1.36**	**1.53**	**1.72**	**1.93**
NA required for Logic, double exposure	**0.62**	**0.72**	**0.82**	**0.95**	**1.06**	**1.19**	**1.34**	**1.50**	**1.68**

193i with water: can do 45nm HP

193i with Gen2 fluid (n=1.65): could enable a ~25nm HP imaging with double exposure

Memory k1=0.28, Logic k1=0.32, Double exposure k1=0.2
Fluid index scaling assumes 0.93NA highest for air

Lithography Technology Requirements

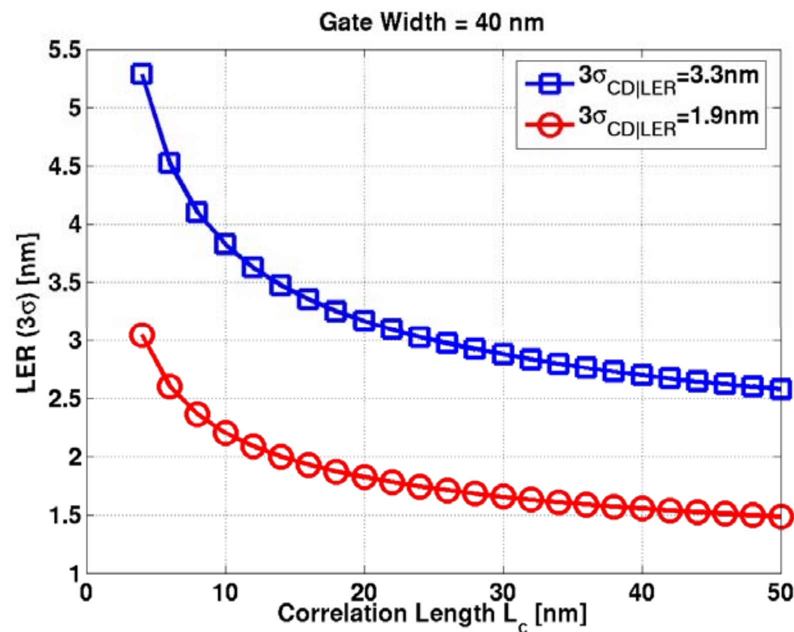
Year of Production	2007	2010	2013	2016	2019	2022
DRAM ½ pitch (nm) (contacted)	**65**	**45**	**32**	**22**	**16**	**11**
DRAM and Flash						
DRAM ½ pitch (nm)	**65**	**45**	**32**	**23**	**16**	**11**
Flash ½ pitch (nm) (un-contacted poly)	**54**	**36**	**25**	**18**	**13**	**9**
Contact in resist (nm)	**70**	**50**	**35**	**25**	**18**	**12.4**
Contact after etch (nm)	**64**	**45**	**32**	**23**	**16**	**11.3**
Overlay [A] (3 sigma) (nm)	**13**	**9.0**	**6.4**	**4.5**	**3.2**	**2.3**
CD control (3 sigma) (nm) [B]	**6.8**	**4.7**	**3.3**	**2.3**	**1.7**	**1.2**
MPU						
MPU/ASIC Metal 1 (M1) ½ pitch (nm)	**68**	**45**	**32**	**23**	**16**	**11**
MPU gate in resist (nm)	**42**	**30**	**21**	**15**	**11**	**8**
MPU physical gate length (nm) *	**25**	**18**	**13**	**9**	**6**	**4**
Contact in resist (nm)	**84**	**56**	**39**	**28**	**20**	**14**
Contact after etch (nm)	**77**	**51**	**36**	**25**	**18**	**13**
Gate CD control (3 sigma) (nm) [B] **	**2.6**	**1.9**	**1.3**	**0.9**	**0.7**	**0.5**

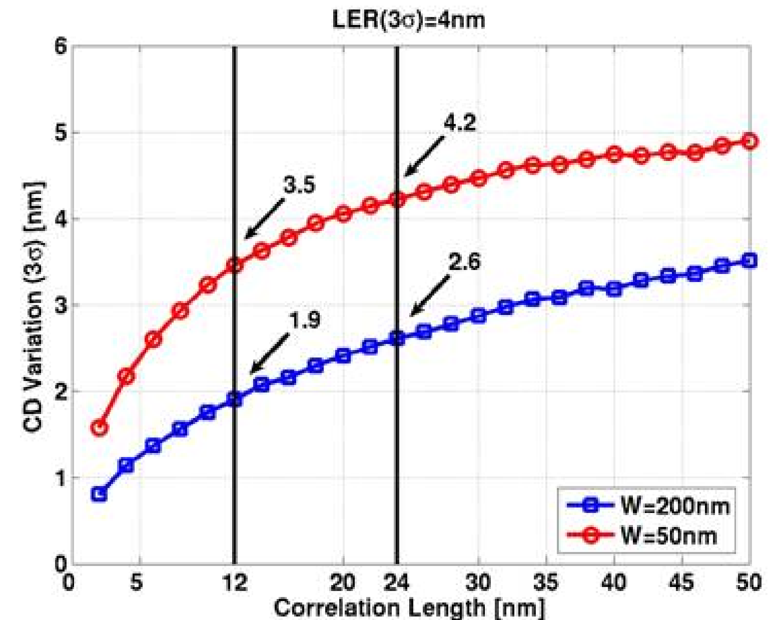
CD Uniformity

- Gate CD uniformity remains orange in 2007 and red next year
  - Gate CDU is 12% of final etched gate size
- Literature reports have demonstrated CDU ~1.3nm (3σ)
  - One wafer, in resist, one pitch, one orientation, excluding mask error
- Contributions to add to match ITRS value:
  - Mask variation, OPC non-correctable error, Wafer-to-wafer, Lot-to-lot, Multiple orientations
- Estimate: Total CDU from adding other components is ~3.2nm
  - Minor change in achievable CDU
  - There is no known solution for the broad definition of all CD uniformity components
  - Most companies practice some level of DFM to achieve their variability targets

LER/LWR Requirement

- LER drives an additional component of CD Uniformity
  - AMD paper
    - "Line Edge Roughness Impact on Critical Dimension Variation," Yuangsheng Ma et al, SPIE 2007
- CD variation increases with smaller gate width
- Required LWR/CD decreases with node
- Included qualitatively in 2007 Chapter text, but not in tables





Overlay

- Overlay: 20% of DRAM half-pitch (not Flash)
  - DRAM drives overlay more so than flash
  - Accelerated Flash schedule would affect ability to hit overlay
    - Overlay is already red for 45nm HP manufacturing
  - Note: most CDU values are driven by tightest half-pitch (flash)
- New data on achieved overlay with immersion lithography presented in October at Immersion Symposium (Keystone, CO) not included in this table update
  - <5nm single-machine overlay, <10nm matched-machine overlay from several vendors
  - ITRS definition is based on use in manufacturing and needs to be discussed in ITRS working groups

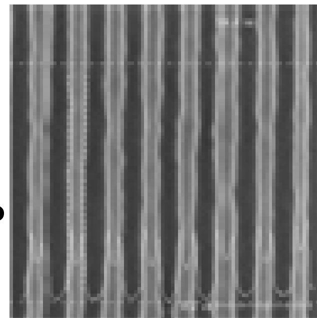
Line Width Roughness

	2007	2010	2013	2016
DRAM ½ pitch (nm)	65	45	32	22
Low frequency line width roughness (nm)	3.4	2.4	1.7	1.2

Industry data does not demonstrate <2.6nm LER/LWR for any current chemically amplified resist system today (at any dose)

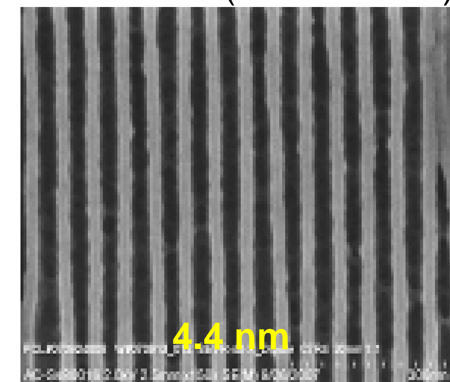
Example 193i resist
From E. Piscani (SEMATECH)

Dipole
40nm HP



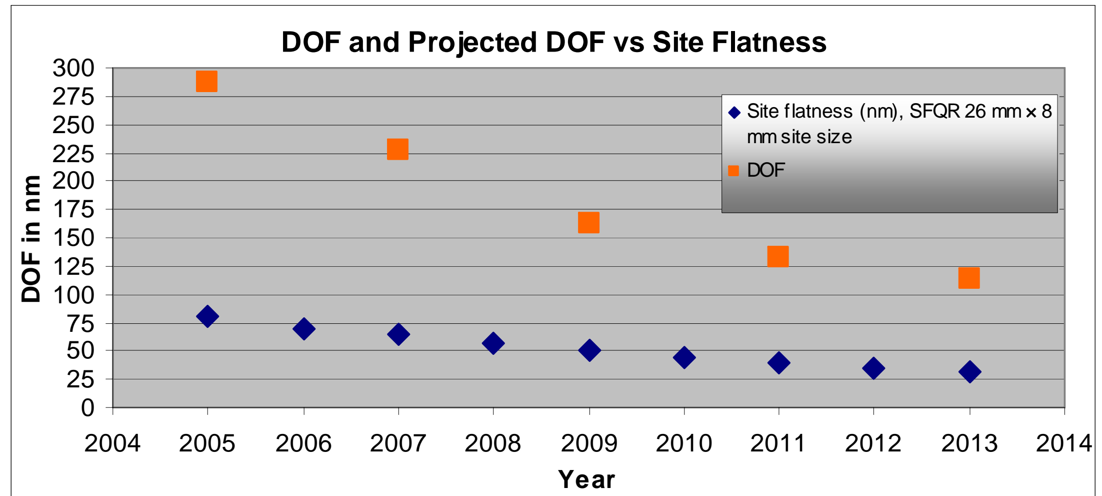
Example EUVL resist
From A. Ma (SEMATECH)

Resist D
Rot-Dipole
30 nm HP



Wafer Flatness Requirement

- 193i at high NA has small DoF
- Need requirement for post-CMP, chucked wafer flatness over 26x8mm scan slit size
  - Only roadmap number today is a bare wafer site flatness requirement



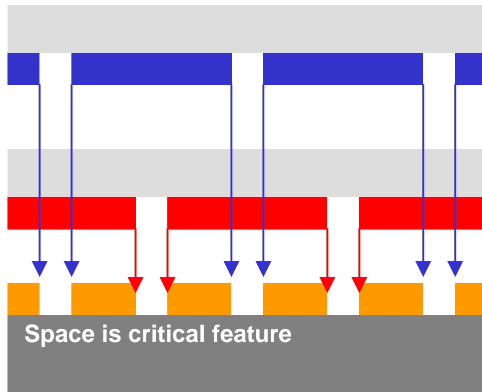
Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
Site flatness (nm), SFQR 26 mm × 8 mm site size	80	70	65	57	45	42	36	35	32
New Site Flatness Targets	80	70	63	54	50	45	40	32	29

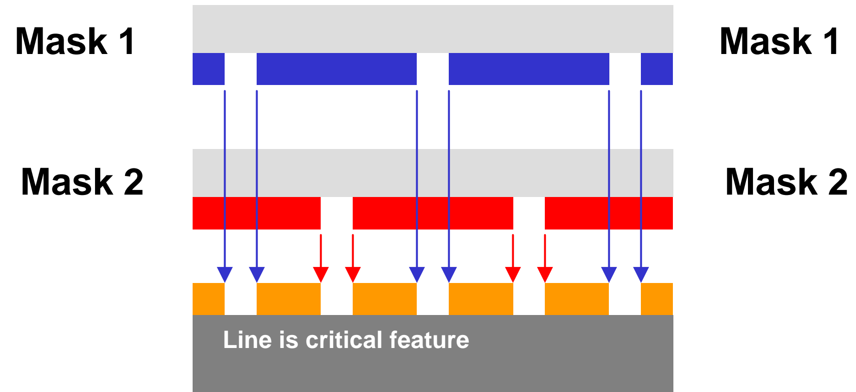
Double Exposure

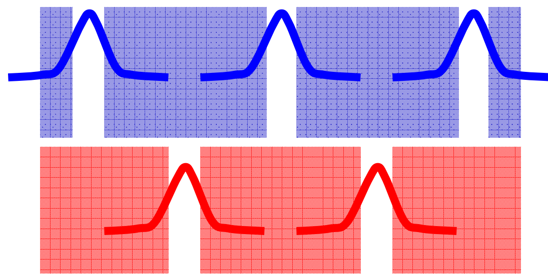
- Simple double exposure: each feature is exposed independently (2006 ITRS)
  - Mask placement tightens by 70%
  - Mean-to-target of mask sets must be matched to within MTT/2
- Defining spaces by dual space exposure (dual space/trench) or defining lines by dual line exposure
  - Adds etch bias uniformity / repeatability
- Defining spaces by dual line exposure or lines by dual space exposure
  - CD of resulting features defined by overlap of two exposures
  - Mask image placement tightens
  - Mask CD 3σ tightens

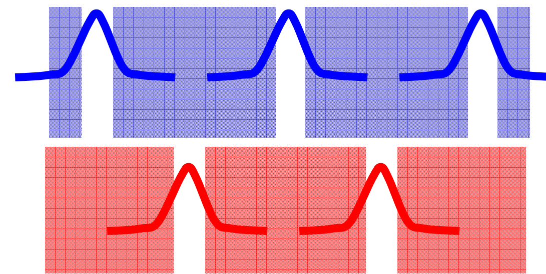
Independent

Dependent

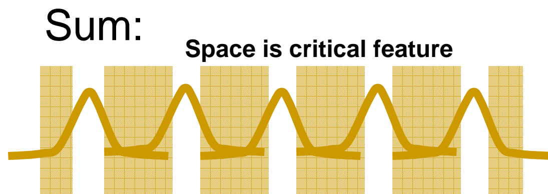


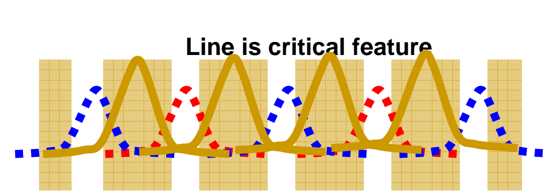






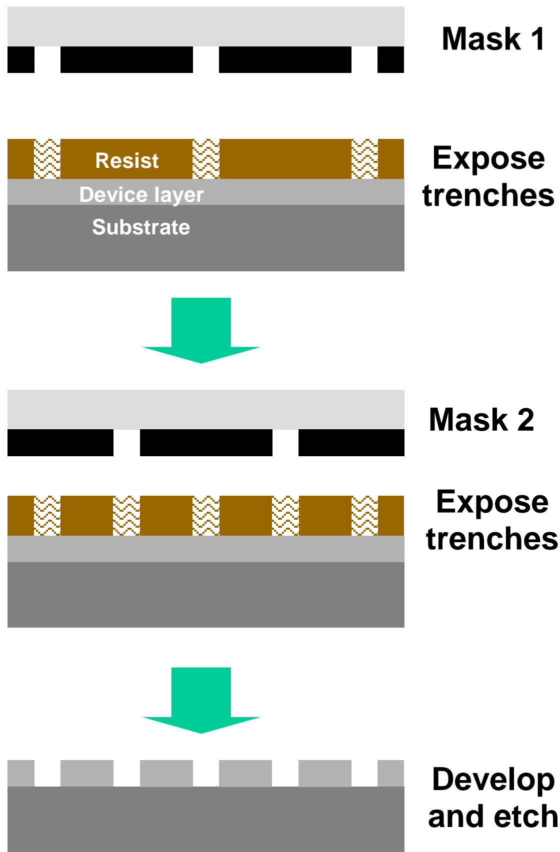
Sum:



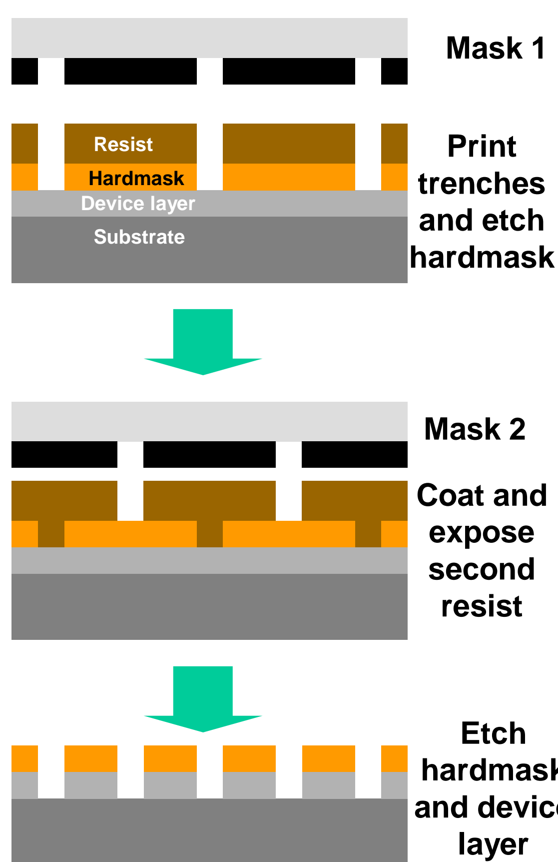


Double Exposure / Patterning Options

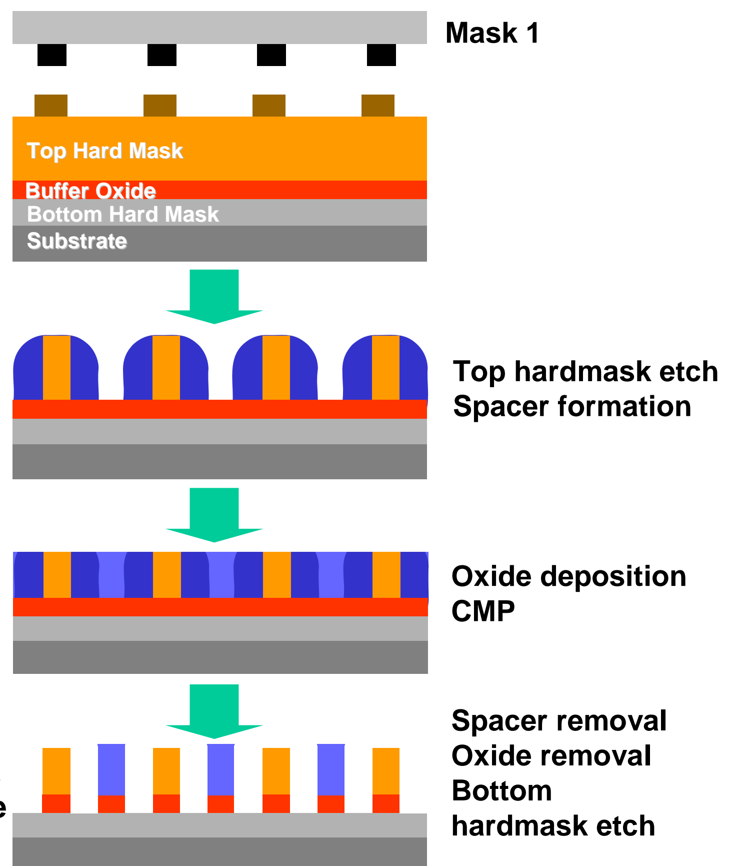
Double Exposure



Double Patterning



Spacer double patterning



2007 Update 193DE/DP

Optical Mask Requirements	*2006*	*2007*	*2010*	*2013*
DRAM HP (nm)	*70*	*65*	*45*	*32*
Image placement for double patterning	**5.7**	**4.9**	**3.4**	**2.4**
Difference in CD Mean-to-target for two masks as a double patterning set	**2.8**	**2.6**	**1.8**	**1.3**
Dual line: mask image placement	**2.5**	**2.3**	**1.6**	**1.2**
Dual line: mask CD 3s	**2.5**	**2.3**	**1.6**	**1.2**
Dual space: repeatability and uniformity of etch bias for double patterning	**1.6**	**1.4**	**1.0**	**0.7**
Spacer PEE process: thickness deviation of deposited layer	To be included in 2008			
Spacer PEE process: thickness uniformity of deposited layer				

Footnote: generic case covers dual space double exposure and patterning but not dual line

Outlook for 2008

- Potential solutions
  - Active discussion on viable solutions for 32nm half-pitch
  - Revisit requirements for extending EUVL to <22nm
  - SEMATECH Litho Forum (May 2008)
- Double exposure / patterning
  - Rapid evolution of new requirements
  - Inclusion of requirements for spacer double patterning
- Mask requirements
  - Specifications for inverse lithography (?)

Summary

- Lithography potential solutions have been narrowed for 45nm DRAM half-pitch
  - 193nm Water based immersion and double patterning solutions are the only technologies available in time
  - 2008 update will be major decision point for 32nm DRAM half-pitch
- Variability control is becoming one of the largest roadmap concerns
  - No known solutions for gate CD uniformity and Line Width Roughness control
- Double exposure / patterning requires a complex set of parameters when different exposures are used to define single features