International Technology Roadmap for Semiconductors

2007 ITRS ORTC

[12/5 Makuhari Japan ITRS Public Conference]

A.Allan, Rev 0.0 (For IRC Review) 10/29/07

Agenda

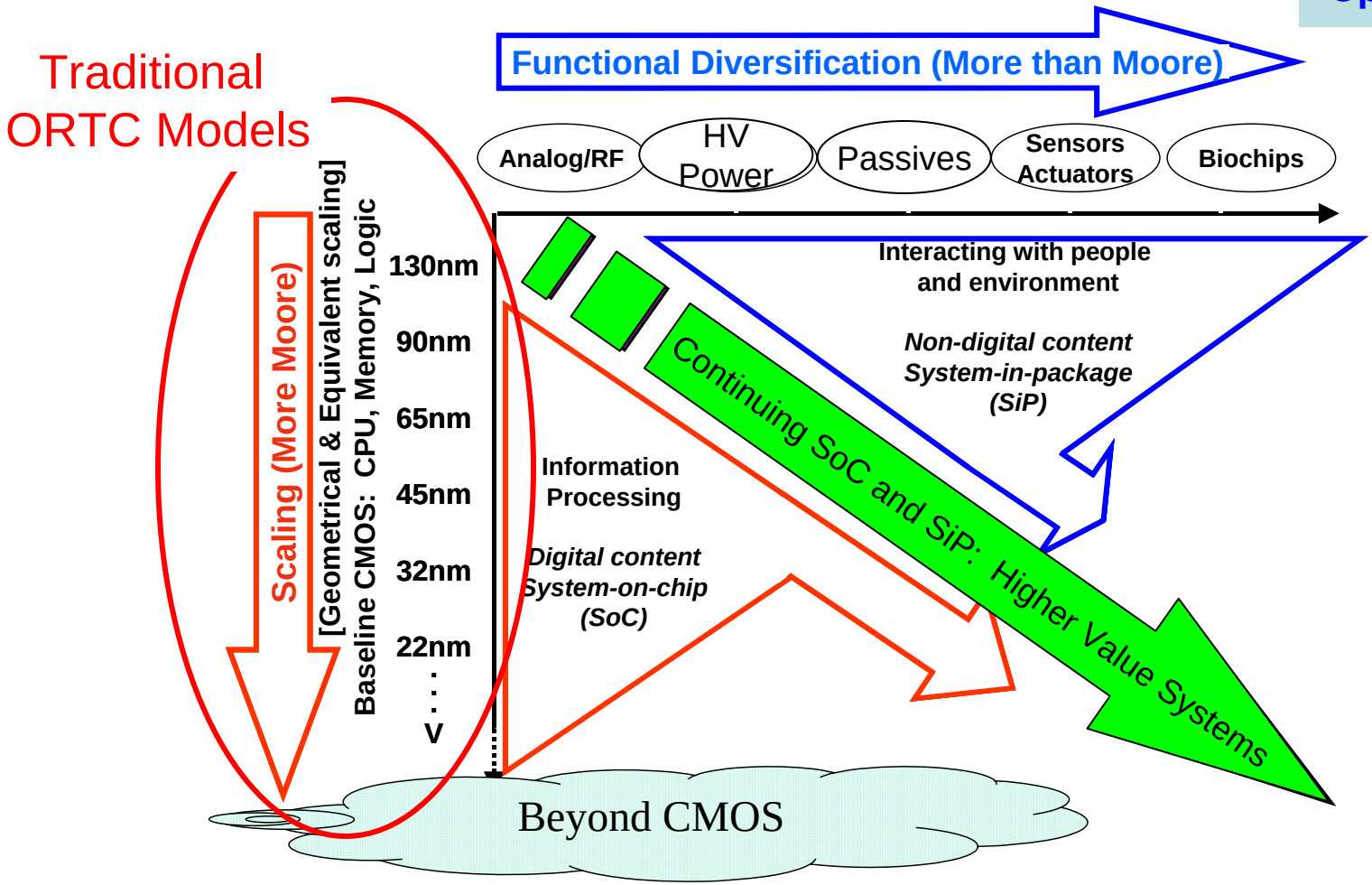
- Moore's Law and More
- Definitions
- Technology Trends Update
- Models Update
  - ITRS Function Size Models
  - ITRS Functions/Chip Models
  - ITRS Chip Size Models
- ITRS Technology Demand Tracking [SICAS]
- Summary

2007 ITRS Executive Summary Fig 5

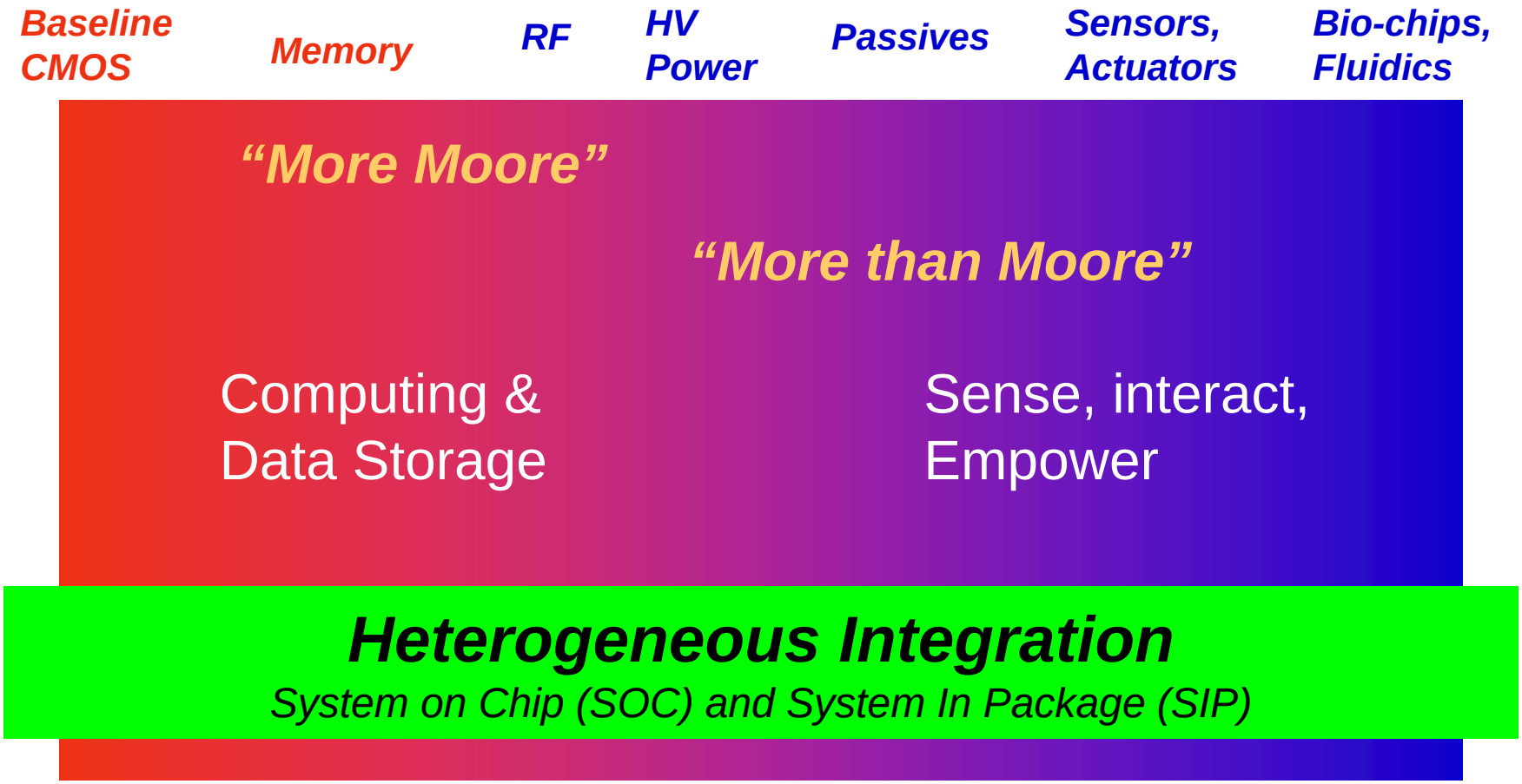
[updated for 2007]

Moore's Law & More

[2007 – add Definitions; Update Graphic]



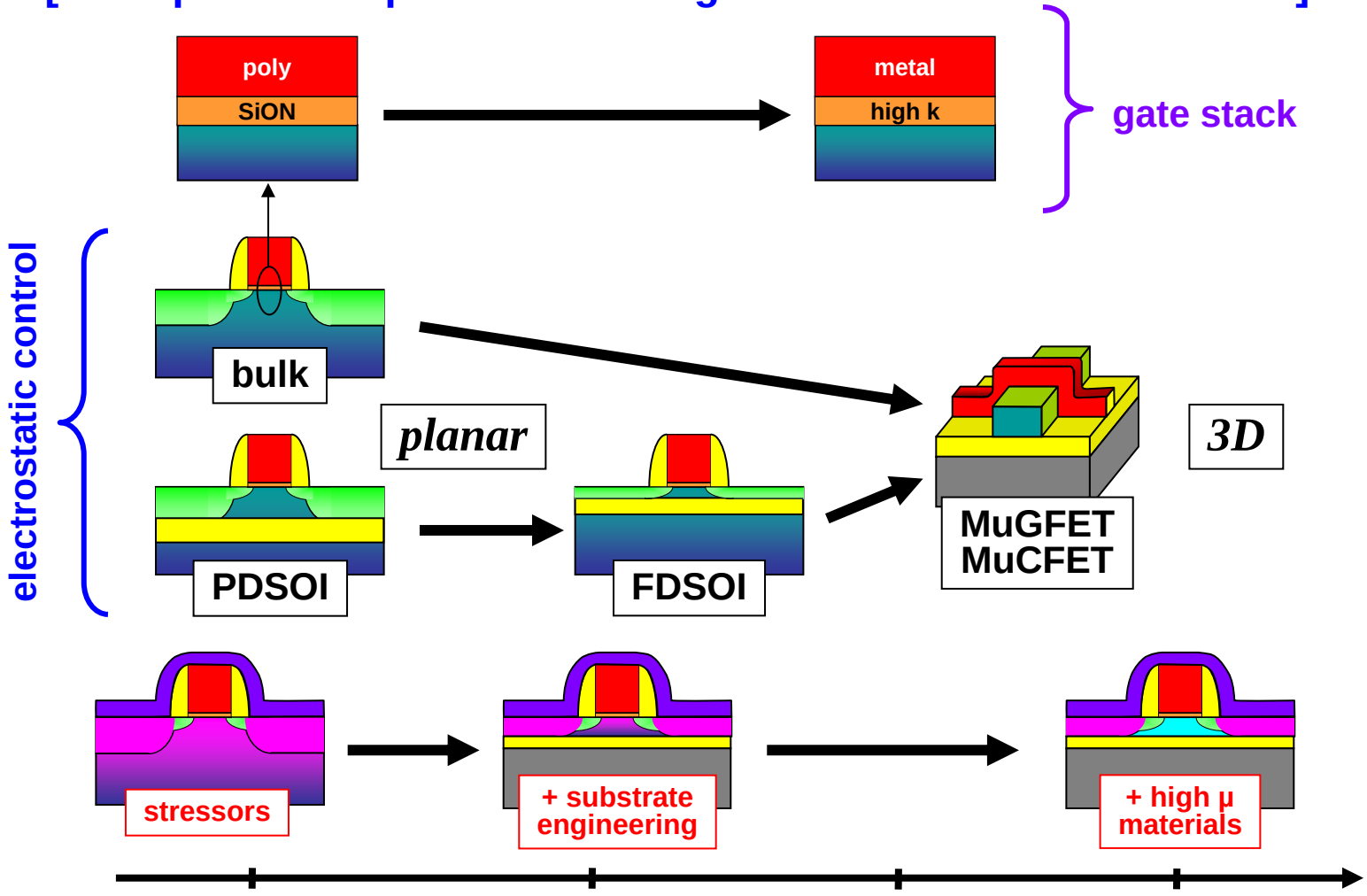
2007 ITRS "Moore's Law and More" Alternative Definition Graphic



Source: ITRS, European Nanoelectronics Initiative Advisory Council (ENIAC)

PIDS/FEP - Simplified Transistor Roadmap

[Examples of "Equivalent Scaling" from ITRS PIDS/FEP TWGs]



[ITRS DRAM/MPU Timing:	2007/7.5	2010	2013	2016]

Source: ITRS, European Nanoelectronics Initiative Advisory Council (ENIAC)

2007 ITRS Definitions: "More Moore" and "More than Moore"

1. **Scaling ("More Moore")**
   a. **Geometrical (constant field) Scaling** refers to the continued shrinking of horizontal and vertical physical feature sizes of the on-chip logic and memory storage functions in order to improve density (cost per function reduction) and performance (speed, power) and reliability values to the applications and end customers.
   b. **Equivalent Scaling** which occurs in conjunction with, and also enables, continued Geometrical Scaling, refers to 3-dimensional device structure ("Design Factor") Improvements plus other non-geometrical process techniques and new materials that affect the electrical performance of the chip.

2. **Functional Diversification ("More than Moore")**

   Functional Diversification refers to the incorporation into devices of functionalities that do not necessarily scale according to "Moore's Law," but provide additional value to the end customer in different ways. The "More-than-Moore" approach typically allows for the non-digital functionalities (*e.g.* RF communication, power control, passive components, sensors, actuators) **to migrate from the system board-level** into a particular package-level (SiP) or chip-level (SoC) potential solution.

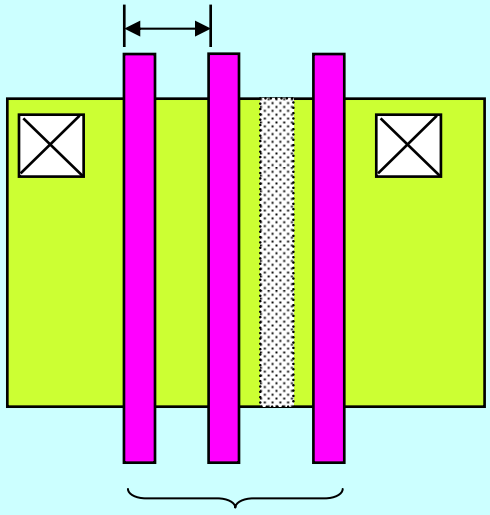
2007 Definition of the Half Pitch - unchanged

[No single-product "node" designation; DRAM half-pitch still litho driver; however, other product technology trends may be drivers on individual TWG tables]

FLASH Poly Silicon ½ Pitch
= Flash Poly Pitch/2

Poly

Pitch



8-16 Lines

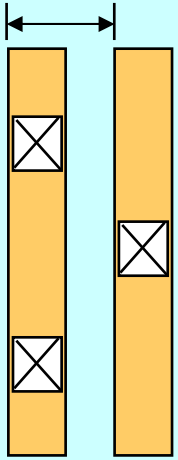
Typical flash
Un-contacted Poly

DRAM ½ Pitch
= DRAM Metal Pitch/2

MPU/ASIC M1 ½ Pitch
= MPU/ASIC M1 Pitch/2

Metal

Pitch



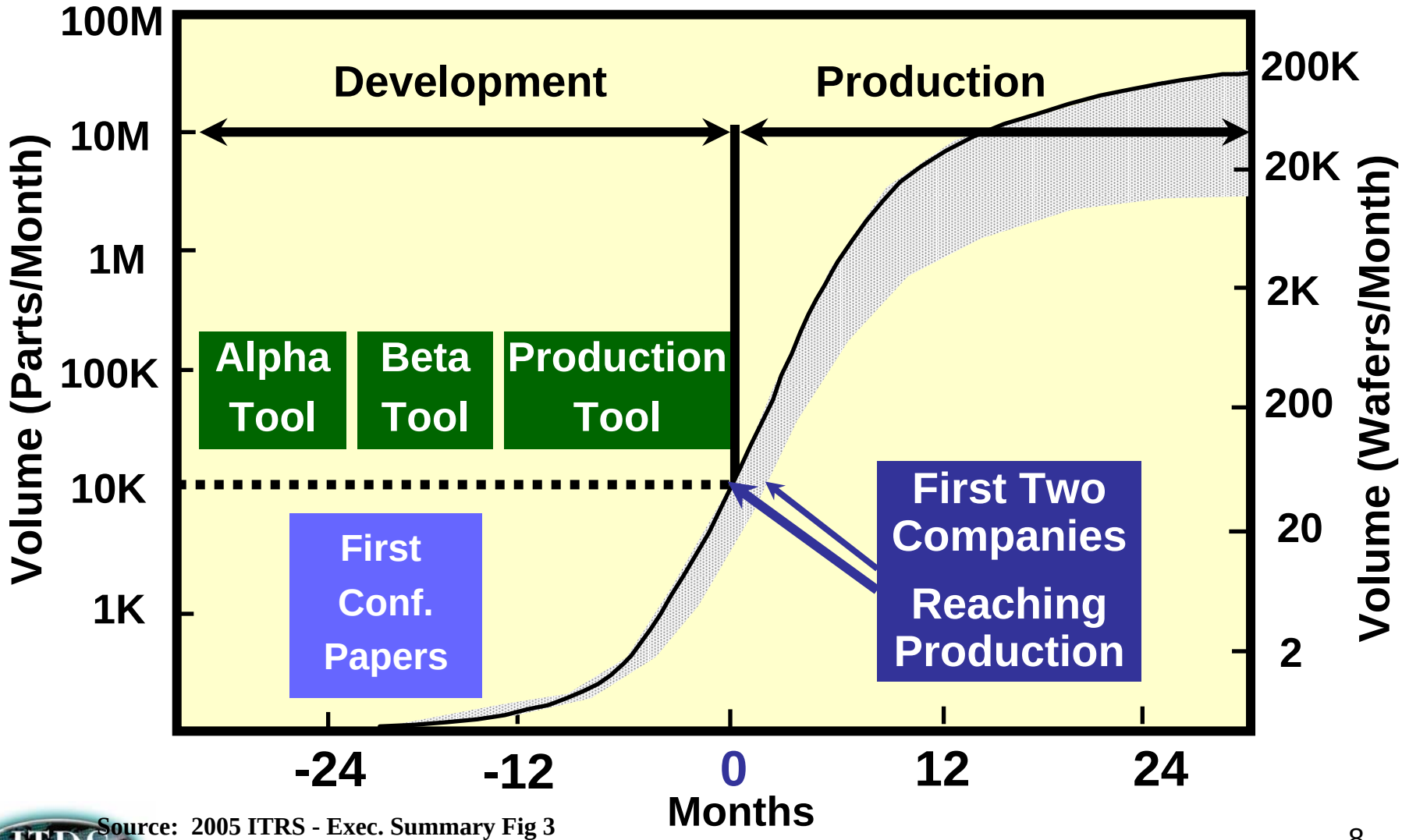
Typical DRAM/MPU/ASIC
Metal Bit Line

Source: 2005 ITRS - Exec. Summary Fig 2

Fig 3

2007 - Unchanged

Production Ramp-up Model and Technology Cycle Timing



Source: 2005 ITRS - Exec. Summary Fig 3

ORTC Overview – **2007** ITRS

Summary of Updates

- ORTC Table 1a,b - Flash Poly (Un-contacted dense lines)
  - 2-year Technology Cycle* (0.5x/4yrs) **Extended to 2008**
  - 180nm/2000; 130nm/2002; 90nm/2004; 65nm/2006; **45nm pull-in to 2008**
  - **Then return to 3-year Technology Cycle* 2 years ahead of DRAM '08-'22**
- DRAM M1 will NO LONGER be the standard TWG table technology header**
  - 2007 ITRS Update DRAM 3-year cycle stagger-contacted **Unchanged,**
  - However, **Bits/chip delayed 1yr; 6f2 2006-2022; 56% Area Efficiency pull-in 2 yrs**
- ORTC Table 1a,b - MPU/ASIC M1 Half-Pitch Trend Unchanged
  - Stagger-contacted, same as DRAM
  - 2.5-year Technology Cycle* (.5x/5yrs)
  - 180nm/2000; 90nm/2005; 45nm/2010(equal DRAM)
  - Then continue on a 3-year Technology Cycle*, equal to DRAM 2010-2020
- ORTC Table 1a,b – MPU/ASIC Printed Gate Length per FEP and Litho TWG ratio relationship to Final Physical Gate Length
  - 2005 ITRS target for (3-year cycle* after 2005 Unchanged.
- **TWG table Product-specific technology trend driver header items, as required by TWGS, will be added in 2007 to individual TWG tables from ORTC Table 1a&b
- Chip Size/Function Size/Density Models [Logic Gate; SRAM Cell; Dram Cell; Flash Cell (SLC, MLC)] are updated and aligned to the latest DRAM and Flash proposals
  - Products: Flash; DRAM; High Performance (hp) MPU; Cost Perf. (cp) MPU; hp ASIC

***Note: Cycle = time to 0.5x linear scaling every two cycle periods ~ 0.71x/ cycle**

2007 ('07-'22) ITRS Technology Trends DRAM M1 Half-Pitch : 3-year cycle

Updated

Year of Production	2000 [Actual]	2001	2002 [Actual]	2003	2004	2005	2006	2007	2008	2009	2010	2012	2013	2015	2016	2018	2019	2020	2022
Technology - Contacted M1 H-P (nm)	180	151	130	107	90	80	71	65	57	50	45		32		22		16	14	11

2-Year Technology Cycle ['98-'04]

3-Year Technology Cycle

2005 ITRS Flash Poly Half-Pitch Technology: 2.0-year cycle until 2yrs ahead of DRAM @ 45nm/'08

Year of Production	2000 [Actual]	2001	2002 [Actual]	2003	2004	2005	2006		2008	2009	2010	2012	2013	2015	2016	2018	2019	2020	2022
Technology - Uncontacted Poly H-P (nm)	180	151	130	107	90	76	65	57	50	45		32		22		16		13	10
IS:								'07 53	'08 45	'09 40	'10 36	'11 32		'14 22		'17 16		'20 11	

2-Year Technology Cycle ['98-'06]

3-Year Technology Cycle

2005 ITRS MPU M1 Half-Pitch Technology: 2.5-year cycle; then equal DRAM @45nm/2010

Year of Production	2000	2001	2002 [July'02]	2003	2004	2005	2006	2007 [July'08]	2008	2009	2010	2012	2013	2015	2016	2018	2019	2020	2022
Technology - Contacted M1 H-P (nm)	180	157	136 [130]	119	103	90	78	68 [65]	59	52	45		32		22		16	14	11

3-2-Yr Cycle]

2.5-Year Technology Cycle

3-Year Technology Cycle

Figure 8 ITRS Product Technology Trends

[DRAM &, MPU Unchanged; [Flash 2-yr cycle extended] plus extend all to 2022]

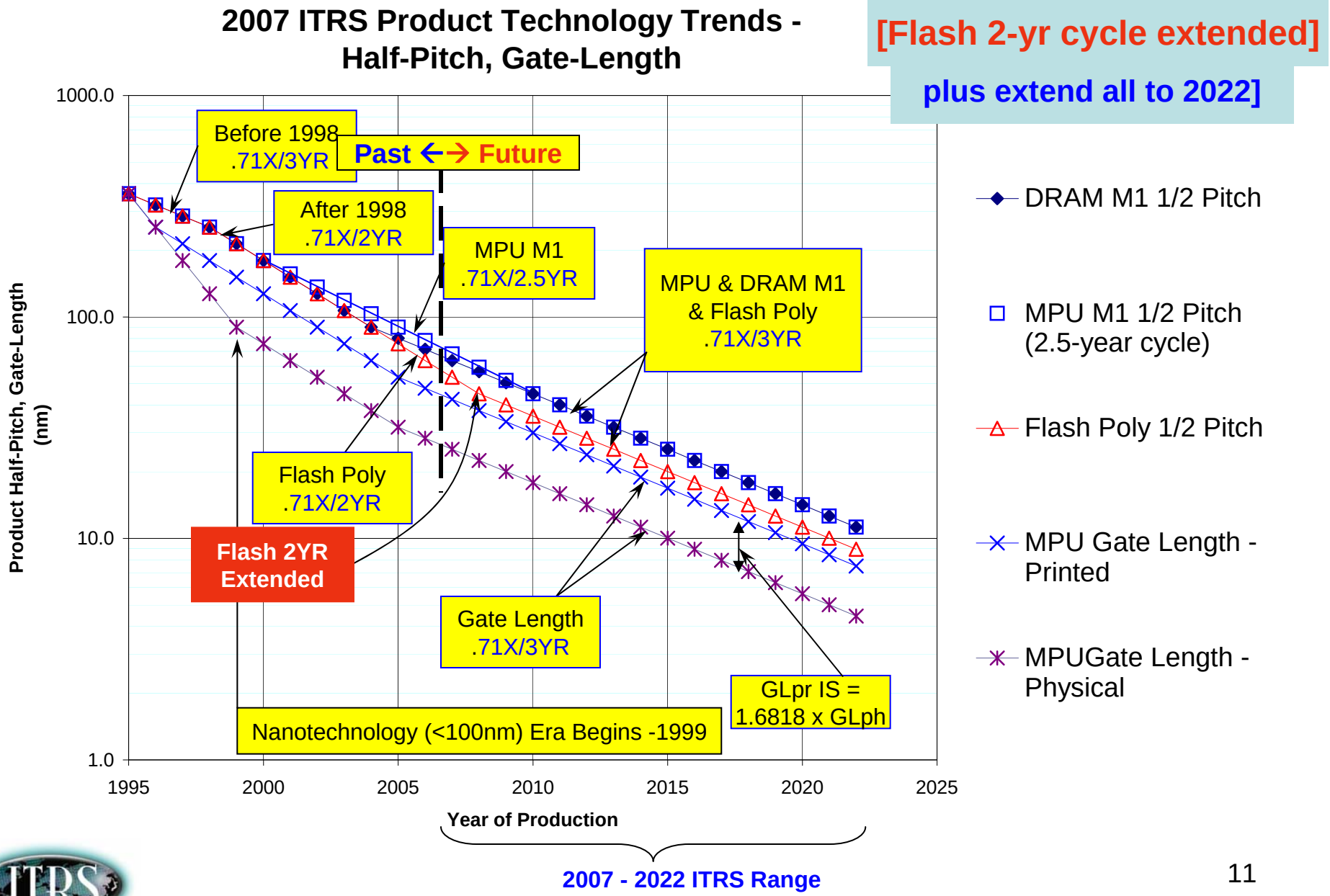
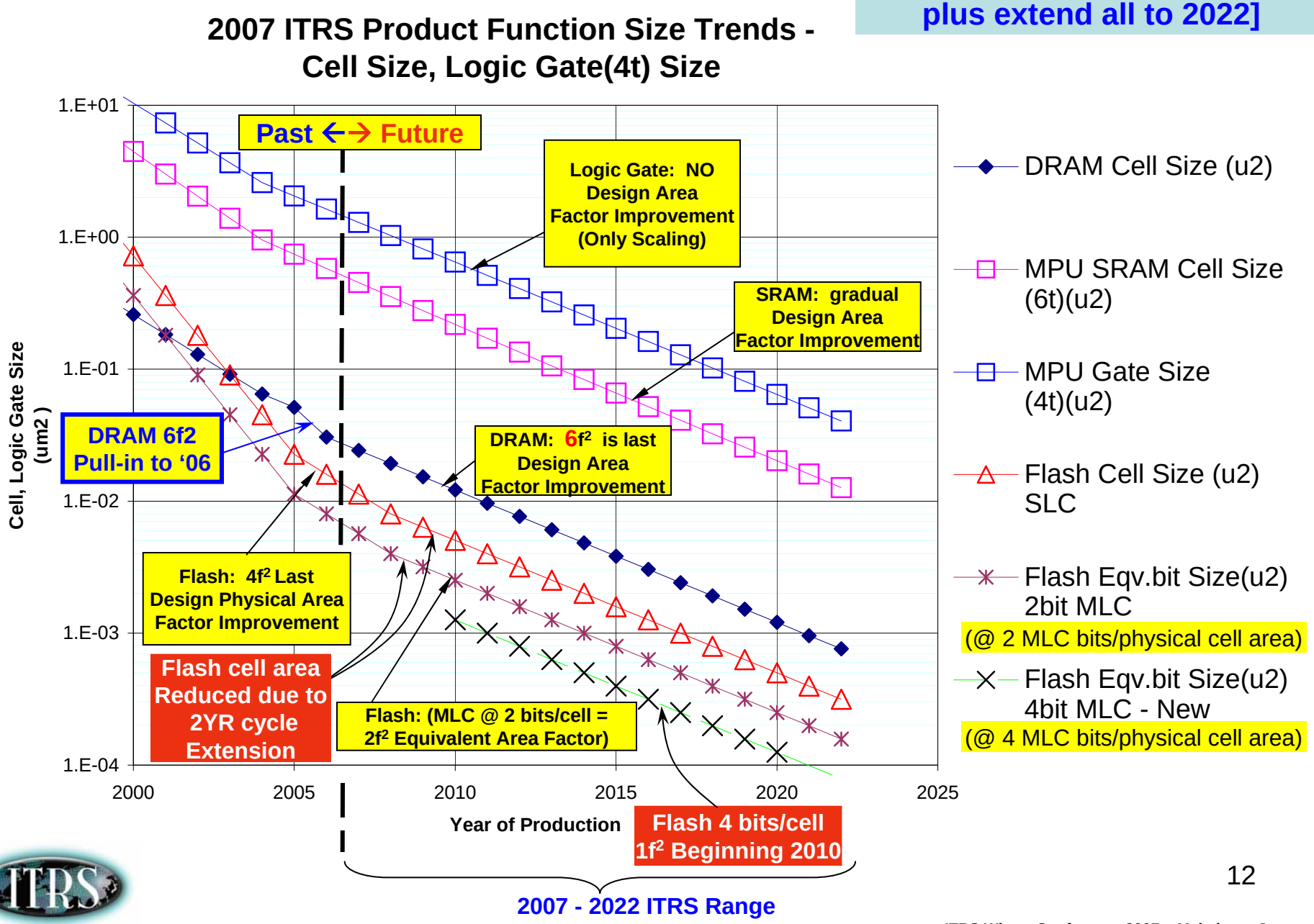


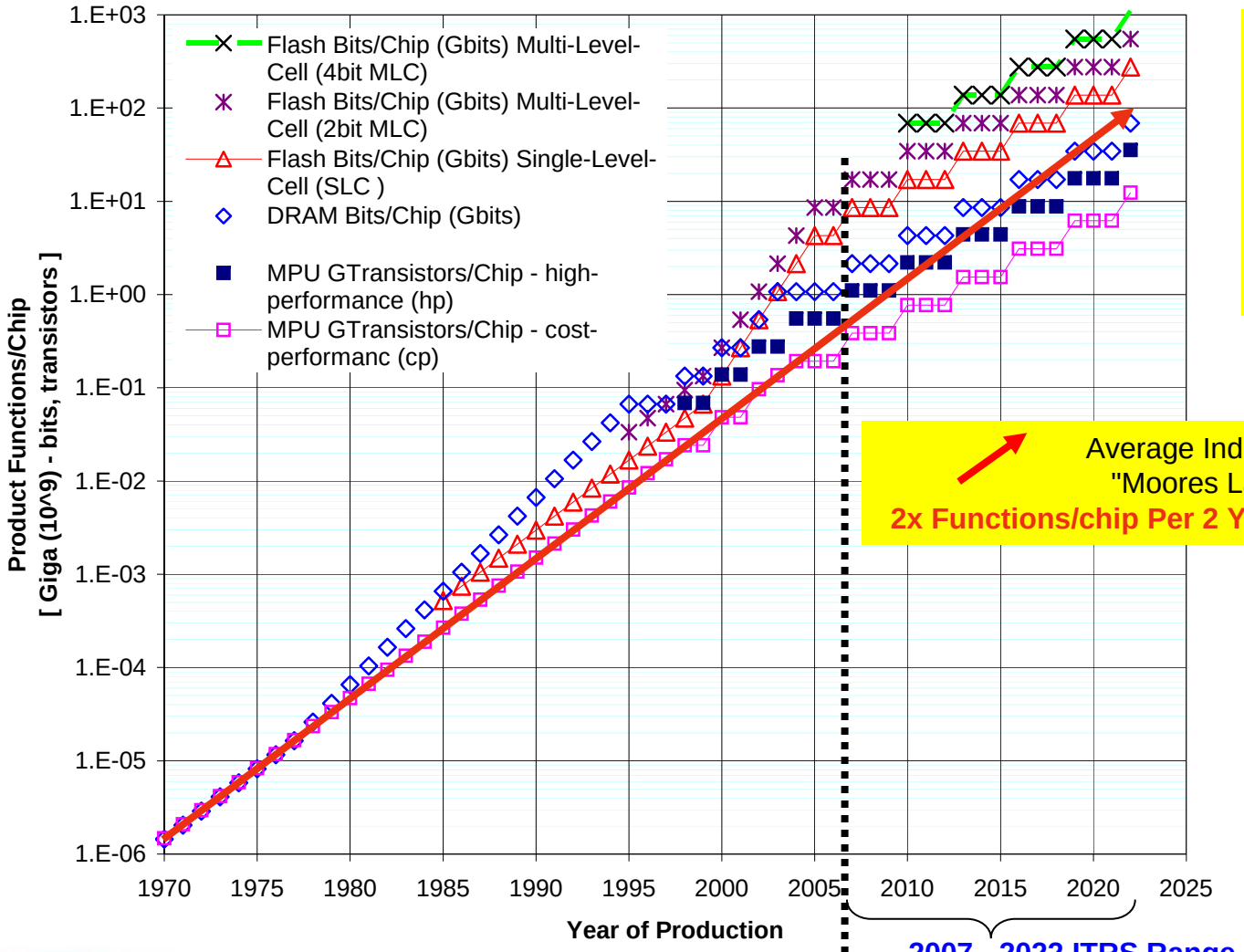
Figure 9 ITRS Product Function Size

[changes to DRAM and Flash; plus extend all to 2022]



Chip Size Trends – 2007 ITRS Functions/Chip Model

2007 ITRS Product Technology Trends - Functions per Chip (@Volume Production, Affordable Chip Size**)



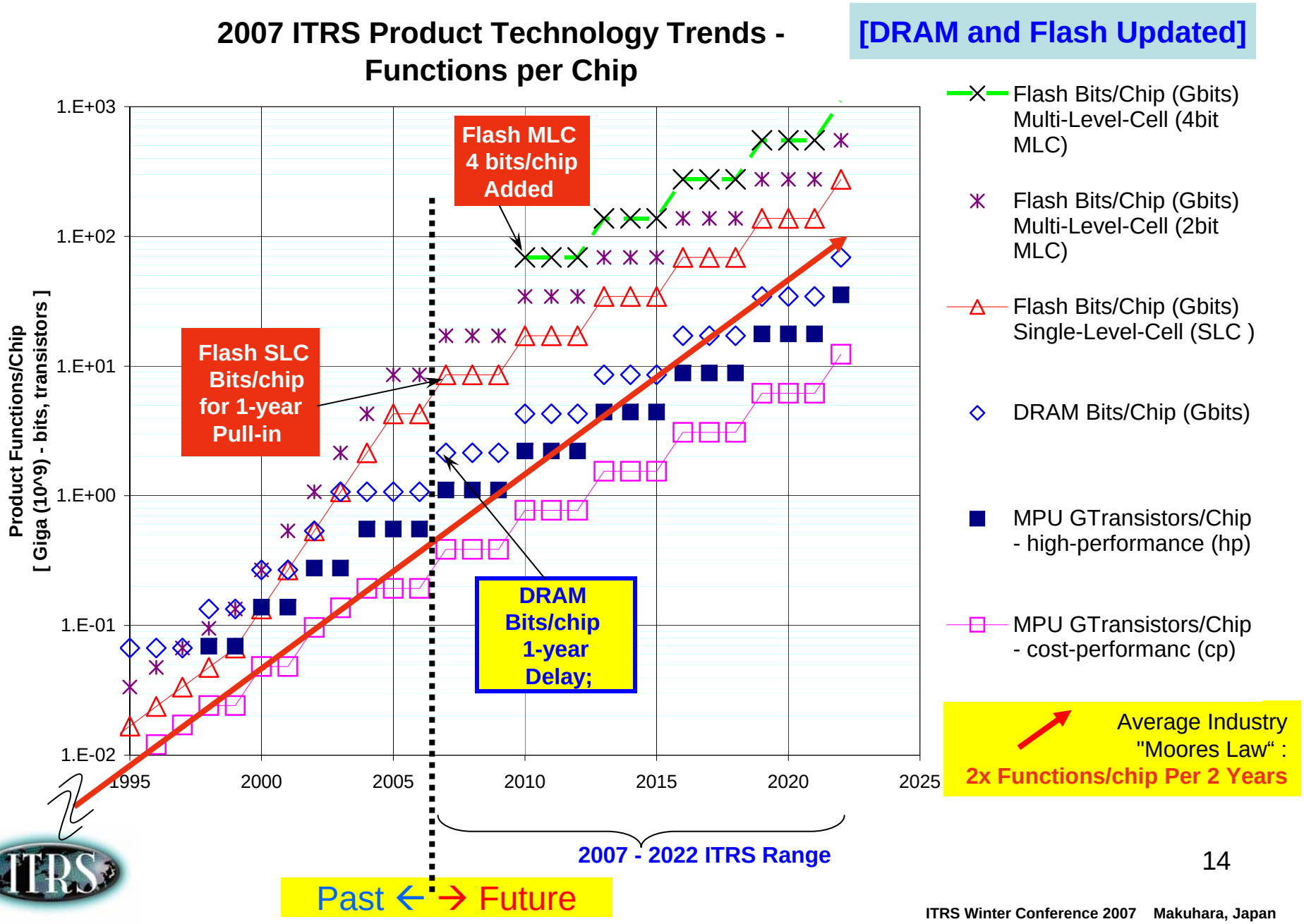
** Affordable Production
Chip Size Targets:
DRAM, Flash < 145mm^2
hp MPU < 310mm^2
cp MPU < 140mm^2

MPU ahead or = "Moore's Law"
2x Xstors/chip
Per 2 years
Thru 2010

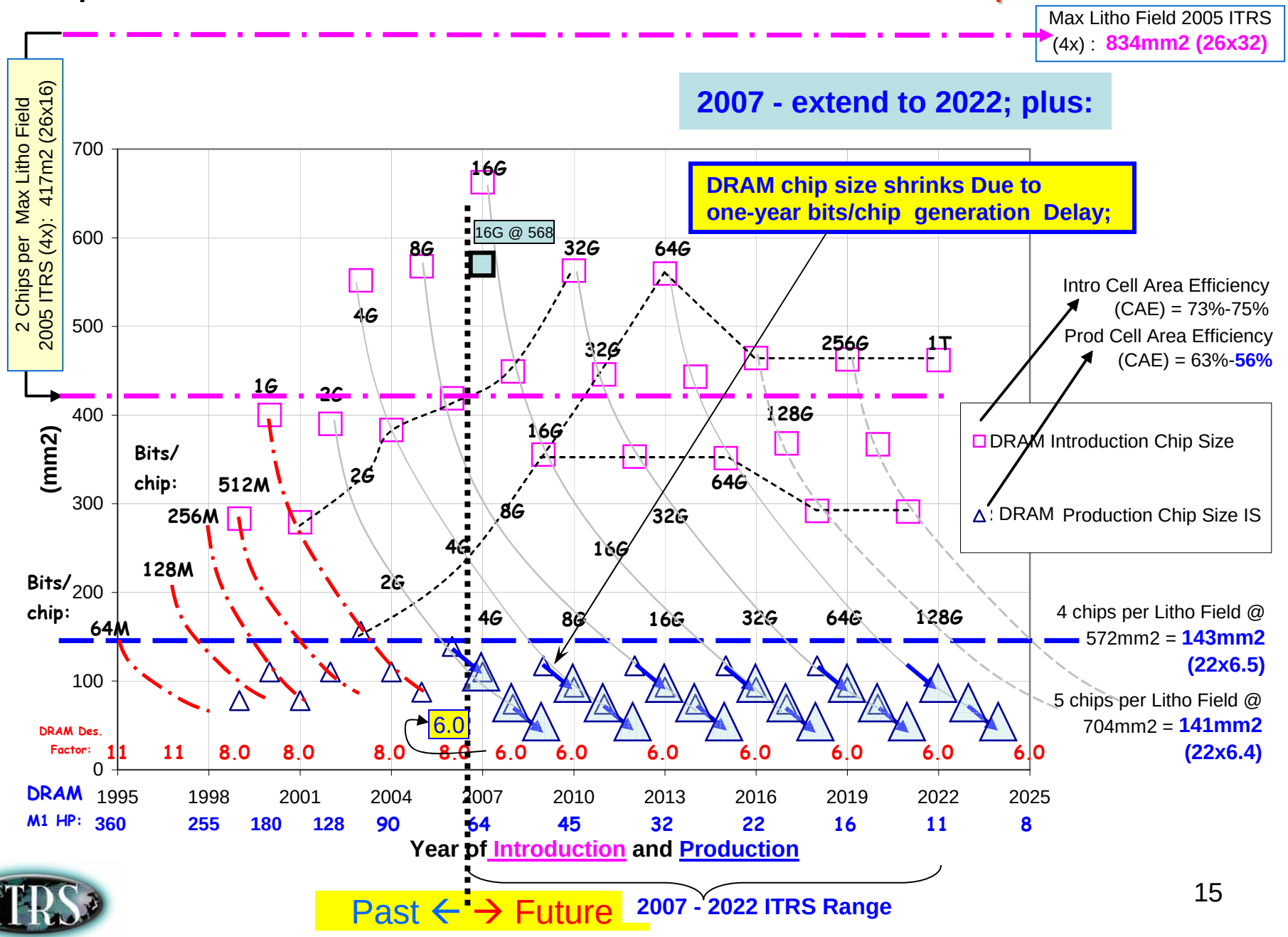
** Example
Chip Size Targets:
1.1Gt P07h MPU
@ intro in 2004/620mm^2
@ prod in 2007/310mm^2

** Example
Chip Size Targets:
0.39Gt P07c MPU
@ intro in 2004/280mm^2
@ prod in 2007/140mm^2

Figure 10 ITRS Product Functions per Chip

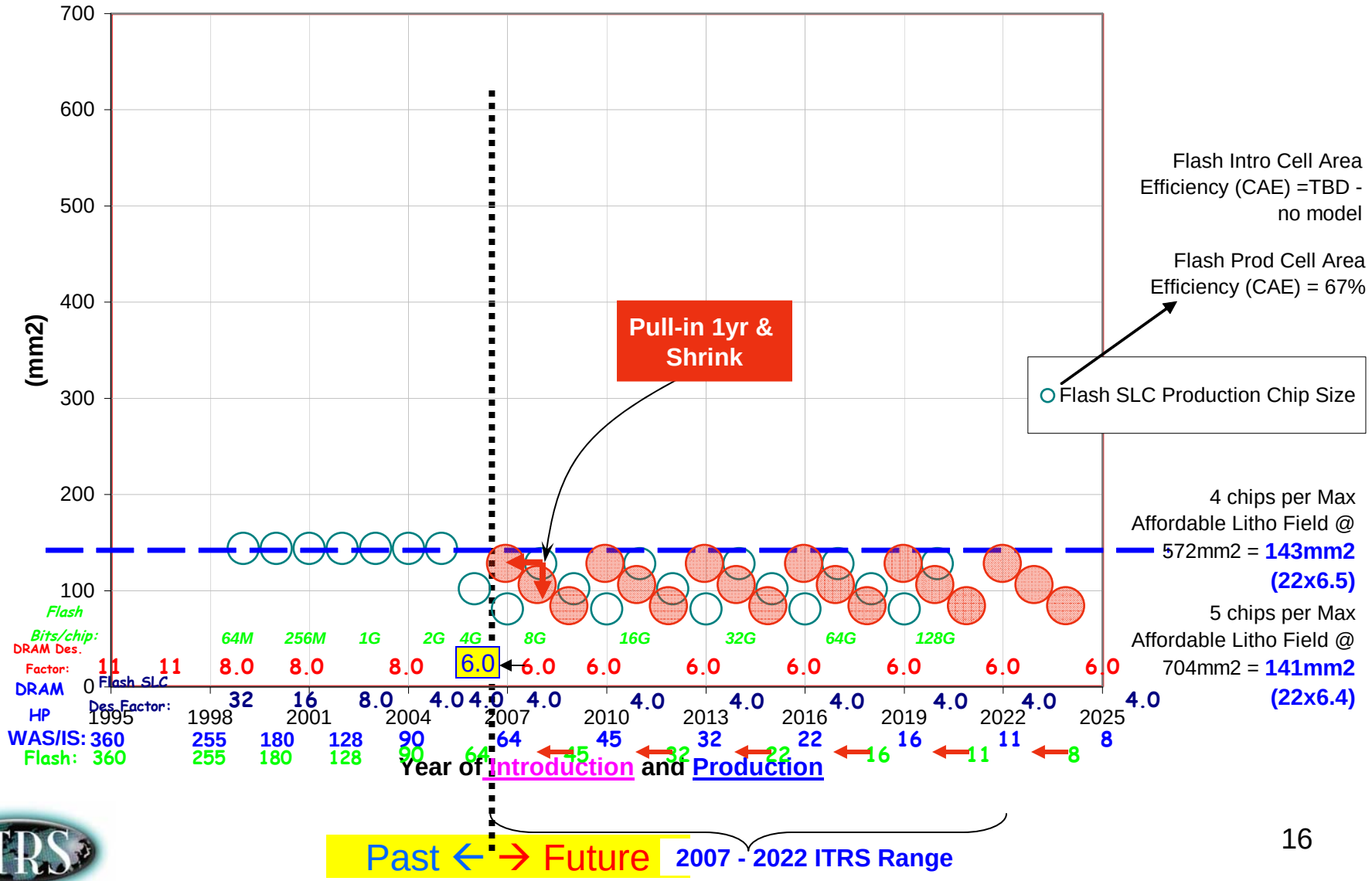


Chip Size Trends – 2005 ITRS DRAM Model – Updated



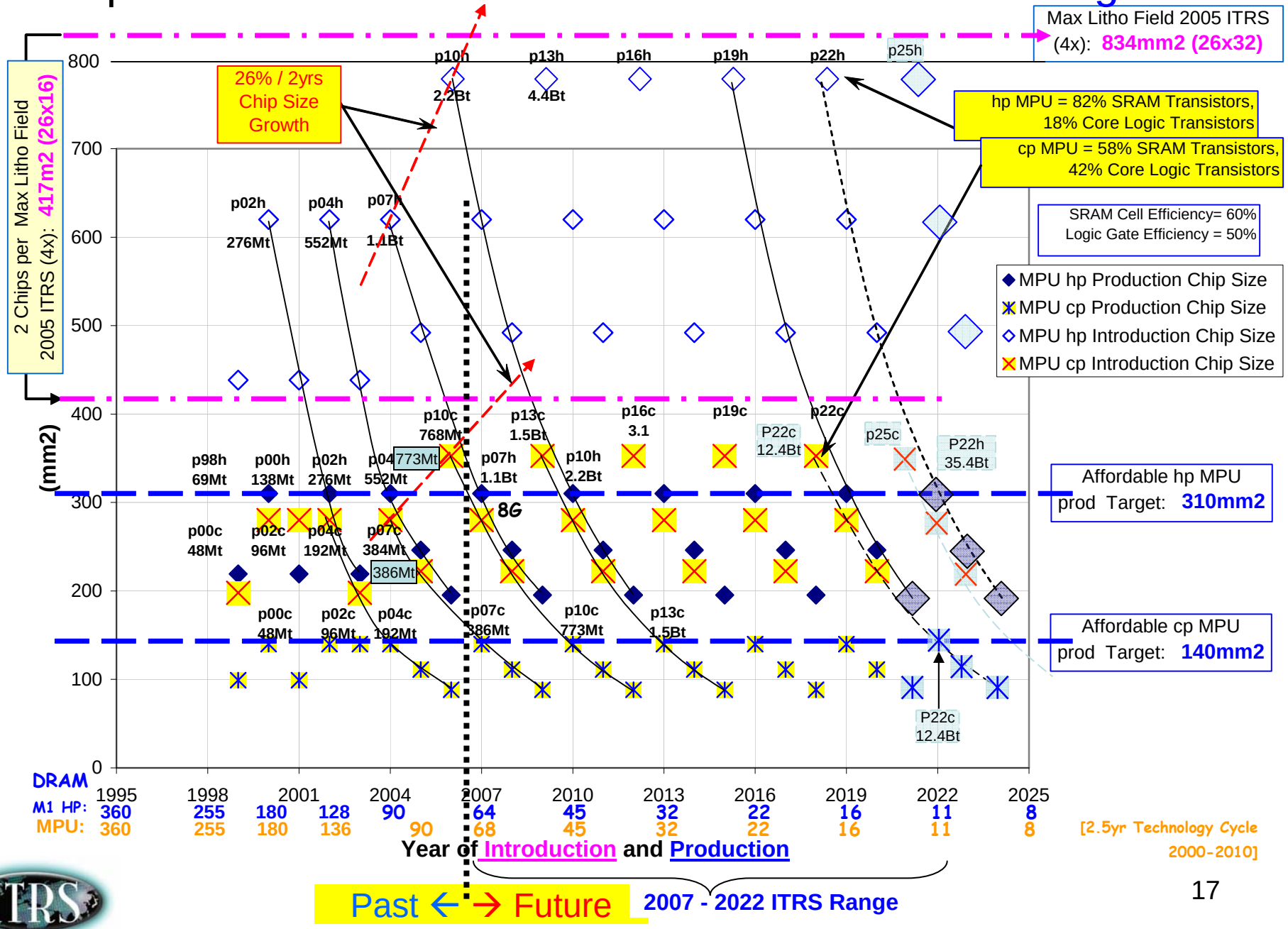
Chip Size Trends – 2005 ITRS Flash Model - Updated

[2007 - extend to 2022]

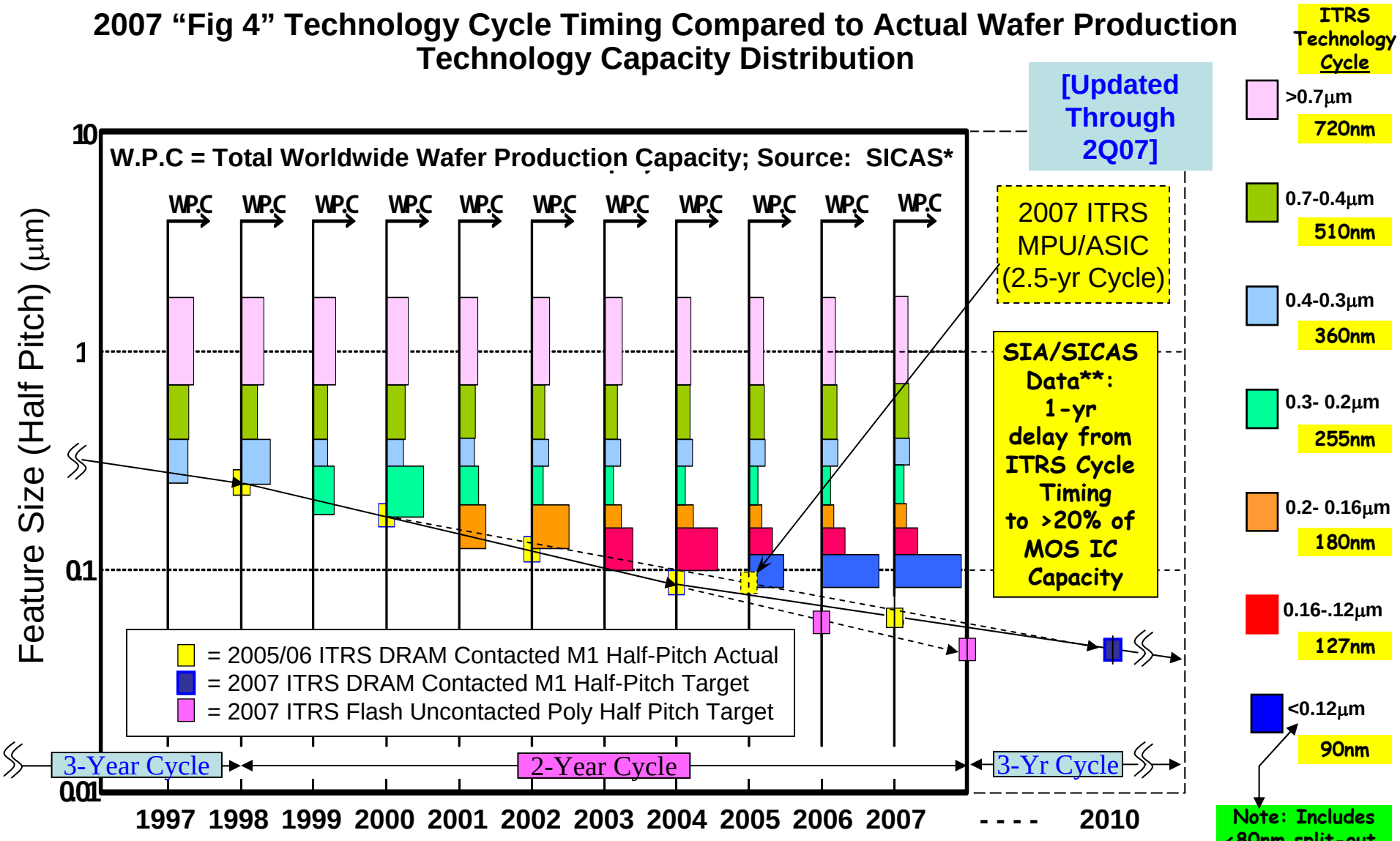


Chip Size Trends – 2005 ITRS MPU Model - unchanged

[2007 - extend to 2022]



2007 "Fig 4" Technology Cycle Timing Compared to Actual Wafer Production Technology Capacity Distribution

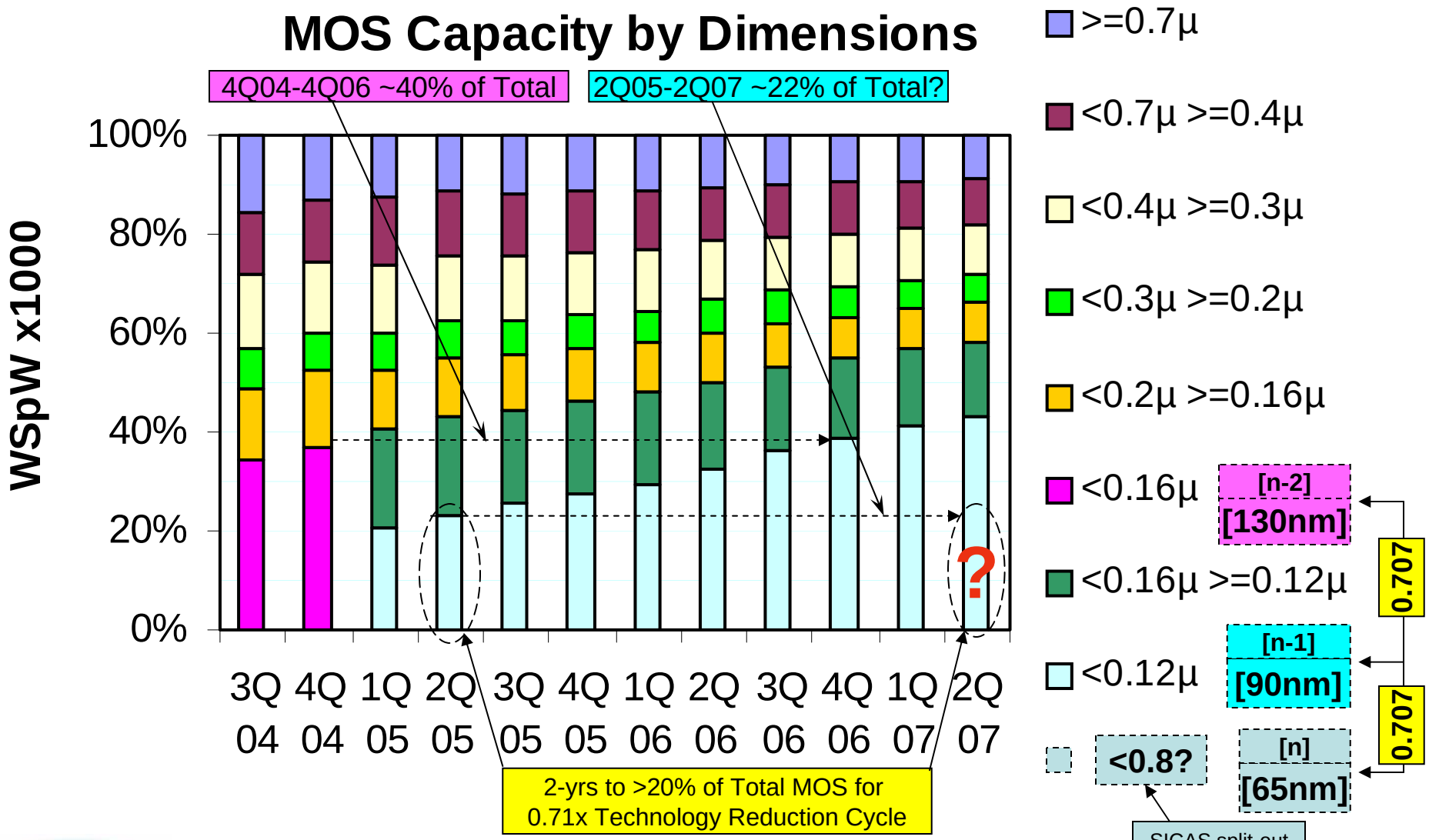


Note: The wafer production capacity data are plotted from the Semiconductor Industry Association (SIA) Semiconductor Industry Capacity Statistics (SICAS) 4Q data for each year, except 2Q data for 2007.
The width of each of the production capacity bar corresponds to the MOS IC production start silicon area for that range of the feature size (y-axis). Data are based upon capacity if fully utilized.

** *Source: The data for the graphical analysis were supplied by the Semiconductor Industry Association (SIA) from their Semiconductor Industry Capacity Statistics (SICAS). The SICAS data is collected from worldwide semiconductor manufacturers (estimated >90% of Total MOS Capacity) and published by the Semiconductor Industry Association (SIA), as of August, 2007. The detailed data are available to the public online at the SIA website, http://www.sia-online.org/pre_stat.cfm .*

Will Capacity Demand Remain On A 2-Year Technology Cycle (.71) for <0.8u (65nm)?

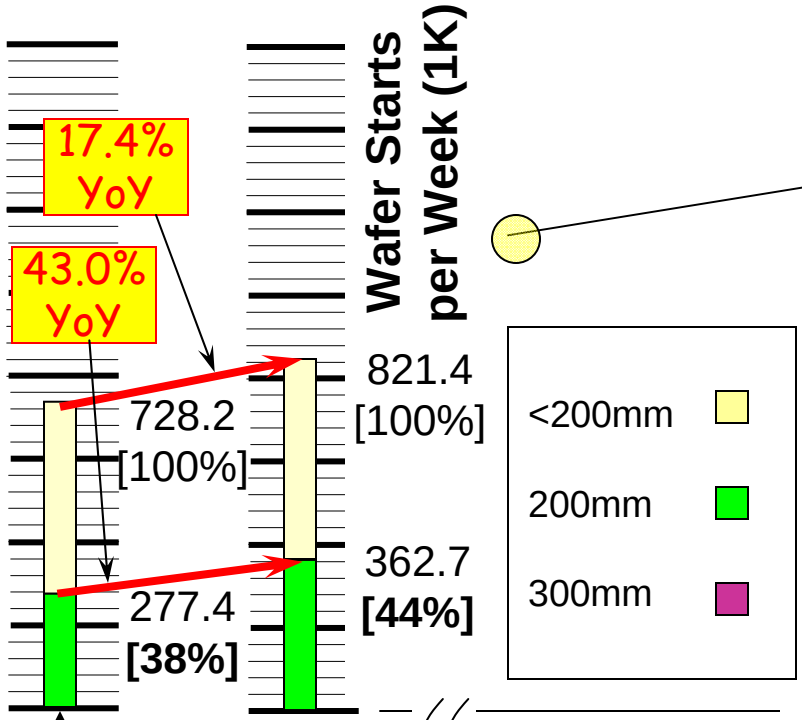
[SICAS Survey November results needed for 2008 Update]



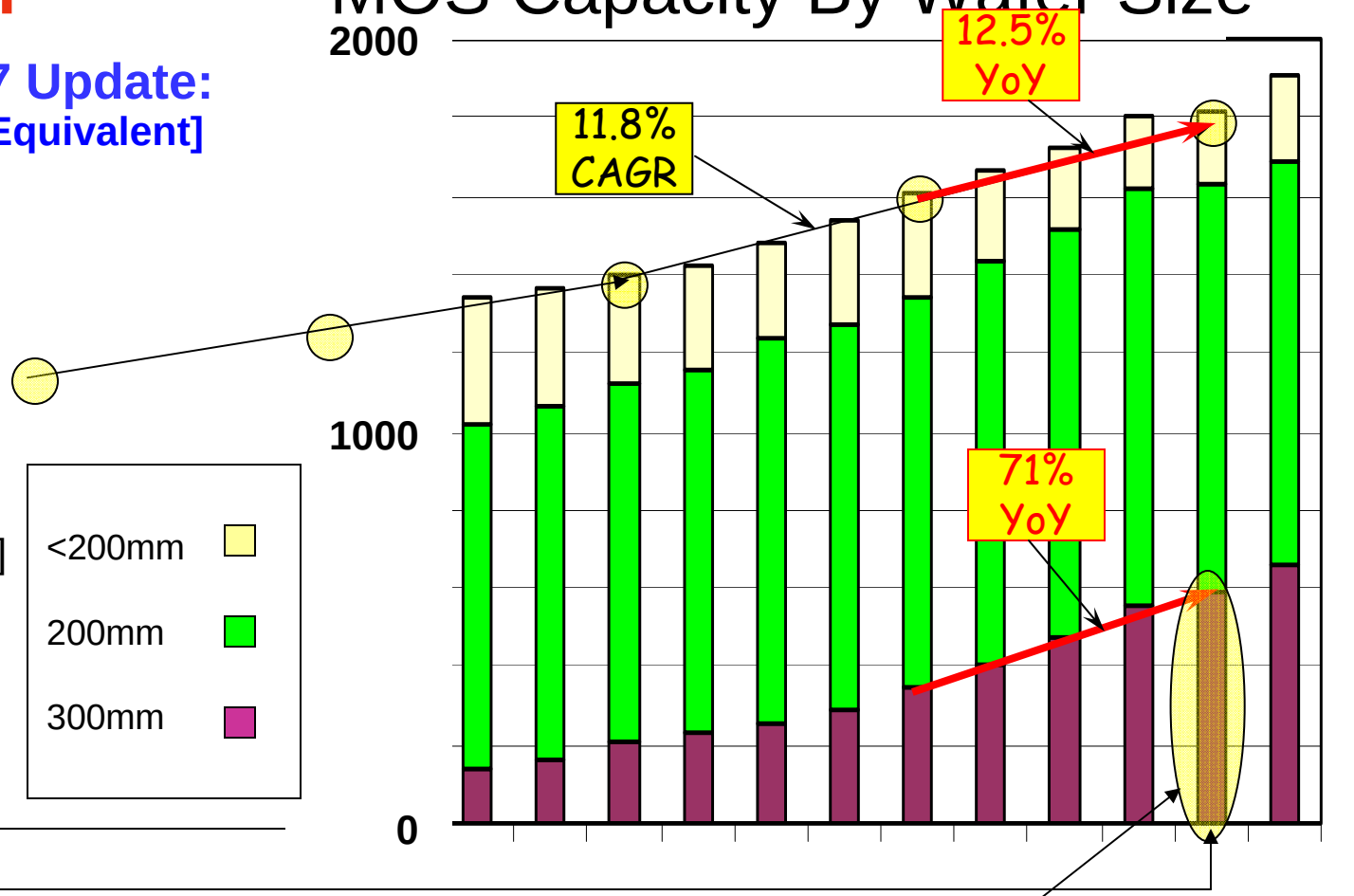
Source: SIA/SICAS Report: www.sia-online.org/pre_statistics.cfm

SICAS 300mm Tracking – 3Q07 Update:

[Total MOS only – 8" Equivalent]



MOS Capacity By Wafer Size



1991->2001: 10 years intro->intro Wafer Generation

200mm/1Q97
SICAS Tracking Begins
(6yrs after Intro)

300mm/1Q04
(3yrs after Intro)

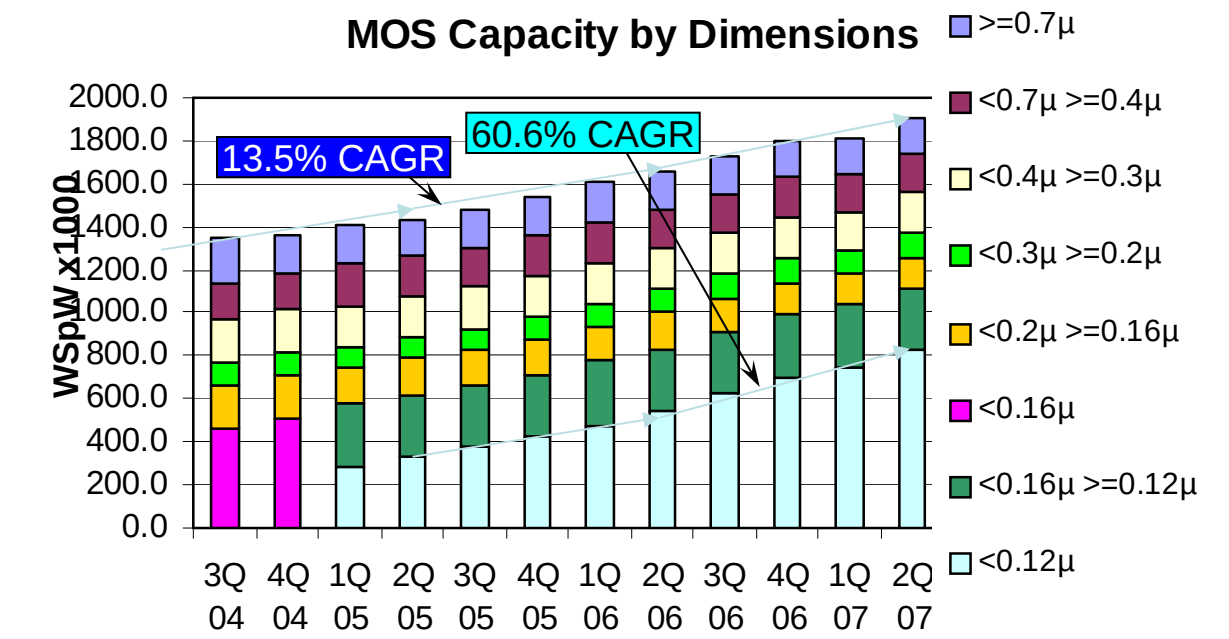
1Q07: 300mm = 33% of Total MOS
200mm = 56% of Total MOS
<200mm = 11% of Total MOS

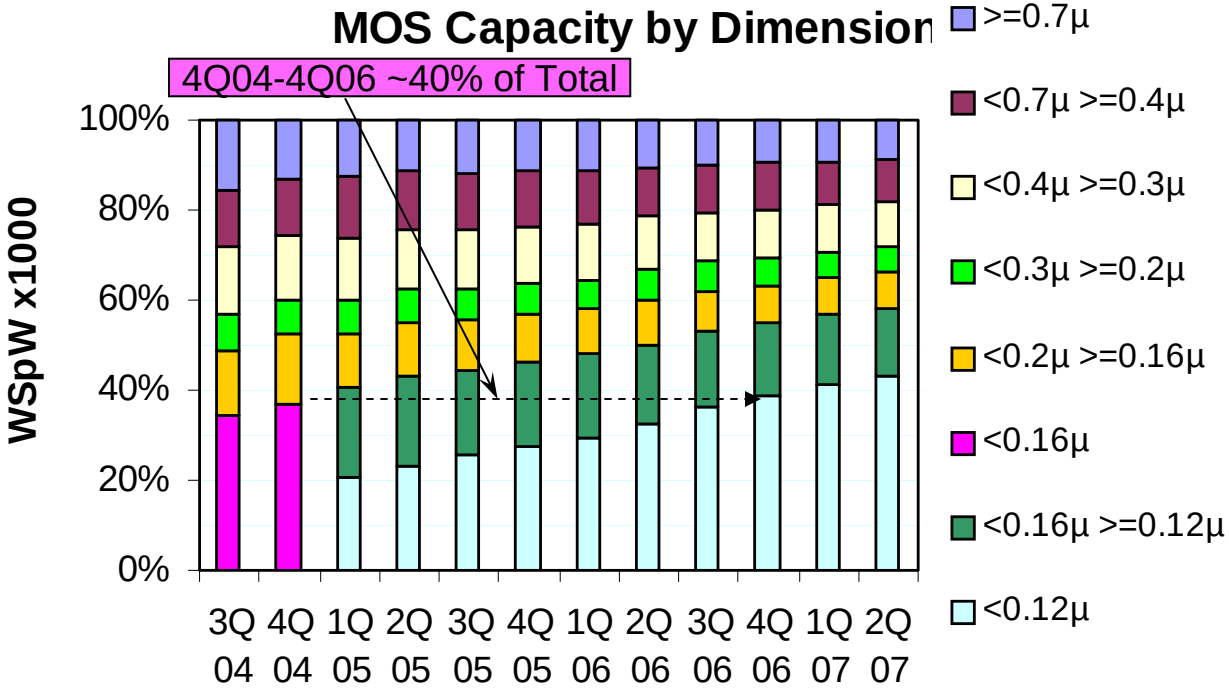
Source: SIA/SICAS Report: www.sia-online.org

ORTC Summary – 2007 Renewal

- Flash Model un-contacted poly half-pitch Extended on 2-year cycle* to 2 years ahead of DRAM (contacted) in 2008, then 3-year cycle*.
- DRAM Model stagger-contacted M1 half-pitch unchanged from 2005 ITRS (3-year cycle* after 2004), however Bits/Chip shifted by one year; 6f2/2006-22 [plus lower Area efficiency 56% pull-in 2 years]
- MPU M1 stagger-contact half-pitch unchanged on a 2.5-year cycle* through 2010/45nm, then 3-year cycle*.
- Printed MPU/ASIC Gate Length FEP and Litho TWGs ratio agreement, and Physical GL targets are both unchanged and on 3-year cycle* beginning 2005.
- New 2007 "Moore's Law and More" Definitions :
  - "Moore's Law" (typically digital computing) Functional and Performance scaling is enabled by both **"Geometrical"** and also **"Equivalent"** scaling technologies
  - "Functional diversification" (typically non-digital sensing, interacting) system board-level migration/miniaturization is enabled by system-in-package and system-on-chip
- Total MOS Capacity (SICAS) has been growing ~12% CAGR (SICAS), and 300mm Capacity Demand has ramped to 33% of Total MOS.
- Historical unchanged chip size models have been updated & "connected" to latest Product scaling rate model proposals, and include design factors, function size, and array efficiency targets
- The average of the industry product "Moore's Law" (2x/chip per 2 years) continues to be met throughout the latest 2007-2022 ITRS timeframe

  [* ITRS Cycle definition = time to .5x linear scaling every two cycle periods]
- Industry Technology Capacity (SICAS) [3Q07 published status] continues on a on 2-year cycle rate at the leading edge.





Source: SIA/SICAS Report: www.sia-online.org/pre_statistics.cfm